ABSTRACT OF THE DISCLOSURE

Within a multi-processing system including a plurality of processor cores 4, 6 operating in accordance with coherent multi-processing, each of the cores includes a cache memory 10, 12 storing local copies of data values from a coherent memory region. The respective processor cores may be placed into a power saving mode in which they are non-operative whilst the cache memory remains responsive to coherency management requests such that the system as a whole can continue to operate and manage coherency.

[Figure 5]